WE CLAIM:

1. A system for verifying connections established through a switching unit adapted to receive a plurality of input signals and output a plurality of switched signals, comprising:

a selection unit for controllably admitting individual ones of the input signals and individual ones of the switched signals; and

a verification unit connected to the selection unit, for controlling operation of the selection unit as a function of a connection map and performing relative-delay-dependent signal processing operations on the signals admitted by the selection unit so as to identify connections established through the switching unit and determine their consistency with the connection map.

2. A system as claimed in claim 1, wherein the connection map defines, for each input signal, a particular one of the switched signals that is expected to be correlated with that input signal, the verification unit being operable to perform the steps of:

causing the selection unit to admit, together with each input signal, the switched signal expected to be correlated with that input signal;

processing the pair of admitted signals to determine a level of correlation or anti-correlation therebetween; and

if the level of correlation is significant or the level of anti-correlation is insignificant, concluding that the connection involving the admitted input signal is consistent with the connection map.

3. A system as claimed in claim 2, the verification unit being further operable to perform the step of:

if the level of correlation is insignificant or the level of anti-correlation is significant:

(1) causing the selection unit to admit, together with said input signal, a switched signal not expected to be correlated with said input signal;

(2) processing the pair of admitted signals to determine the level of correlation or anti-correlation therebetween;

(3) if the level of correlation is significant or the level of anti-correlation is insignificant, concluding that said input signal has been mis-connected; otherwise:

(3.1) if all switched signals not expected to be correlated with said input signal have been exhausted, concluding that the connection involving said input signal has been lost; otherwise:

(3.1.1) causing the selection unit to admit, together with said input signal, a different switched signal not expected to be correlated with said input signal and repeating steps (2) and (3).

4. A system as claimed in claim 1, wherein the verification unit comprises:

a first sampling unit for sampling the input signal admitted by the selection unit, thereby to create a first sample stream;

a second sampling unit for sampling the switched signal admitted by the selection unit, thereby to create a second sample stream;

a first delay line for receiving the first sample stream, comprising a plurality of taps interspersed by delay elements;

a second delay line for receiving the second sample stream, comprising a plurality of taps interspersed by delay elements;

a plurality of anti-correlators, each having a first input connected to a tap in the first delay line and a second input connected to a tap in the second delay line, each correlator being adapted to produce an anti-correlation value at a distinct relative delay; and

a minimum detector connected to the anti-correlators, for selecting the least among the anti-correlation values produced by the anti-correlators and providing the result to a controller.

5. A system as claimed in claim 4, wherein the first and second sampling units each comprise an anti-alias filter, a sampler and an analog-to-digital converter.

6. A system as claimed in claim 4, wherein each anti-correlator is adapted to produce an anti-correlation value that is a function of the difference between the values of the samples appearing at its first and second inputs.

7. A system as claimed in claim 4, wherein each anti-correlator is adapted to produce an anti-correlation value from an input signal x(i) and a switched signal y(i) that is substantially equal to a moving average value of $(x(i-s)-y(i))^2$, where "s" represents a constant relative delay between the two signals.

8. A system as claimed in claim 1, wherein the verification unit comprises:

a first sampling unit for sampling the admitted input signal, thereby to create a first sample stream;

a second sampling unit for sampling the admitted switched signal, thereby to create a second sample stream;

a first delay line for receiving the first sample stream, comprising a plurality of taps interspersed with delay elements;

a second delay line for receiving the second sample stream, comprising a plurality of taps interspersed with delay elements;

a plurality of correlators, each having a first input connected to a tap in the first delay line and a second input connected to a tap in the second delay line, each correlator being adapted to produce a correlation value; and

a maximum detector connected to the correlators, for selecting the greatest among the correlation values produced by the correlators and providing the result to a controller.

9. A system as claimed in claim 8, wherein the first and second sampling units each comprise an anti-alias filter, a sampler and an analog-to-digital converter.

10. A system as claimed in claim 1, wherein the selection unit comprises an arrangement of at least one first multiplexer for allowing selection of the one or more input signals and at least one second multiplexer for allowing selection of the one or more switched signals.

11. A system as claimed in claim 1, wherein the selection unit comprises means for reducing the bandwidth of the admitted signals relative to the signals entering the selection unit.

12. A system as claimed in claim 1, wherein the selection unit comprises means for causing conversion of the input and switched signals from optical to electrical format.

13. A system as claimed in claim 12, wherein the selection unit comprises circuitry for admitting an input signal as a function of an input wavelength and an input port and for admitting a switched signal as a function of a switched wavelength and a switched port.

14. A system as claimed in claim 1, wherein the relative-delay-dependent signal processing operations are performed on low-frequency portions of the input signals and switched signals.

15. A method of validating connections established through a switching unit adapted to receive a plurality of input signals and output a plurality of switched signals, comprising:

selecting one of the input signals;

on the basis of a connection map, identifying a particular one of the switched signals as expected to be correlated with the selected input signal;

determining a level of correlation or anti-correlation between the selected input signal and the switched signal expected to be correlated with the selected input signal; and

if the level of correlation is significant or the level of anti-correlation is insignificant, concluding that the connection involving the selected input signal is consistent with the connection map.

16. A method as claimed in claim 15, further comprising:

if the level of correlation is insignificant or the level of anti-correlation is significant:

(1) determining the level of correlation or anti-correlation between the selected input signal and a switched signal not expected to be correlated with that input signal;

(2) if the level of correlation is significant or the level of anti-correlation is insignificant, concluding that the selected input signal has been mis-connected; otherwise:

(2.1) if all switched signals not expected to be correlated with the selected input signal have been exhausted, concluding that the connection involving the selected input signal has been lost; otherwise:

(2.1.1) repeating steps (1) and (2) with a different switched signal not expected to be correlated with the selected input signal.

17. A method as claimed in claim 15, wherein selecting one of the input signals includes specifying a port and wavelength associated with the selected input signal and wherein accessing each switched signal by specifying a port and wavelength associated with that switched signal.

18. A method as claimed in claim 15, wherein determining the correlation or anti-correlation between two signals is executed on low-frequency portions of said signals.

19. A method as claimed in claim 15, wherein determining the anti-correlation between two signals x(i) and y(i) comprises evaluating a moving average value of $(x(i-s)-y(i))^2$, where "s" represents a constant relative delay between the two signals.

20. A system for validating connections established through a switching unit adapted to receive a plurality of input signals and output a plurality of switched signals, comprising:

means for selecting one of the input signals;

means for identifying, for each selected input signal and on the basis of a connection map, a particular one of the switched signals as expected to be correlated with the selected input signal;

means for determining a level of correlation or anti-correlation between the selected input signal and the switched signal expected to be correlated with the selected input signal; and

means for concluding that the connection involving the selected input signal is consistent with the connection map if the level of correlation is significant or the level of anti-correlation is insignificant.

21. An apparatus for validating connections established through a switching unit adapted to receive a plurality of input signals and output a plurality of switched signals, comprising:

a mechanism constructed and adapted to select one of the input signals;

a mechanism constructed and adapted to identify, for each selected input signal and on the basis of a connection map, a particular one of the switched signals as expected to be correlated with the selected input signal;

a mechanism constructed and adapted to determine a level of correlation or anti-correlation between the selected input signal and the switched signal expected to be correlated with the selected input signal; and

a mechanism constructed and adapted to conclude that the connection involving the selected input signal is consistent with the connection map if the level of correlation is significant or the level of anti-correlation is insignificant.

22. Computer-readable media tangibly embodying a program of instructions executable by a computer to perform a method of validating connections established through a switching unit adapted to receive a plurality of input signals and output a plurality of switched signals, the method comprising:

selecting one of the input signals;

on the basis of a connection map, identifying a particular one of the switched signals as expected to be correlated with the selected input signal;

determining a level of correlation or anti-correlation between the selected input signal and the switched signal expected to be correlated with the selected input signal; and

if the level of correlation is significant or the level of anti-correlation is insignificant, concluding that the connection involving the selected input signal is consistent with the connection map.

23. At least one computer programmed to execute a process for validating connections established through a switching unit adapted to receive a plurality of input signals and output a plurality of switched signals, the process comprising:

selecting one of the input signals;

on the basis of a connection map, identifying a particular one of the switched signals as expected to be correlated with the selected input signal;

determining a level of correlation or anti-correlation between the selected input signal and the switched signal expected to be correlated with the selected input signal; and

if the level of correlation is significant or the level of anti-correlation is insignificant, concluding that the connection involving the selected input signal is consistent with the connection map.

24. A switch for optical signals, comprising:

a switching core for switching a plurality of input optical signals as a function of a connection map and outputting a plurality of switched optical signals; and

a connection verification system connected to the switching core, for correlating the input optical signals with the switched optical signals so as to determine the consistency of the connections established through the switching core with the connection map.

25. A switch as claimed in claim 24, wherein the switching core comprises:

a plurality of optical switch matrices, each optical switch matrix dedicated to a distinct wavelength and having a plurality of inputs and a plurality of outputs, each optical switch matrix being adapted to establish wavelength-preserving connections between its inputs and its outputs.

25. A switch as claimed in claim 24, further comprising:

a plurality of wavelength division demultiplexing (WDD) devices, each having an input port and a plurality of output ports;

a plurality of wavelength division multiplexing devices, each having an output port and a plurality of input ports; and

wherein the inputs of each optical switch matrix are connected to the like-wavelength output ports of the WDD devices; and

wherein the outputs of each optical switch matrix are connected to the like-wavelength input ports of the WDM devices.

26. A switch as claimed in claim 25, wherein the connection verification system is coupled to the inputs of the WDD devices and to the outputs of the WDM devices.

27. A switch as claimed in claim 26, wherein the connection map is defined by a set of sub-maps including a sub-map for each optical switch matrix defining a desired interconnection pattern between the inputs of that optical switch matrix leading from the WDD devices and the outputs of that optical switch matrix leading to the WDM devices, and wherein the connection verification system comprises:

a first selection unit for controllably extracting single-carrier input signals from among the signals leading from the inputs of the WDD devices;

a second selection unit for controllably extracting single-carrier switched signals from among the signals leading from the outputs of the WDM devices; and

a verification unit connected to the first and second selection units, for controlling operation of the first and second selection units as a function of the sub-maps and performing relative-delay-dependent signal processing operations on the signals extracted by the selection units so as to identify connections established by each optical switch matrix and to determine their consistency with the associated sub-map.

28. A switch as claimed in claim 25, wherein the switching core further comprises a wavelength converting switch having a plurality of inputs and a plurality of outputs, the inputs of the wavelength converting switch being connected to a subset of the outputs of each optical switch matrix and the outputs of the wavelength converting switch being connected to a subset of the inputs of each optical switch matrix.

29. A switch as claimed in claim 28, wherein the connection verification system is coupled to the outputs of the WDM devices and to those inputs of each optical switch matrix connected to outputs of the wavelength converting switch.

30. A switch as claimed in claim 29, wherein the connection map is defined by a set of sub-maps including a sub-map for each optical switch matrix defining a desired interconnection pattern between the inputs of that optical switch matrix leading from the wavelength converting switch and the outputs of that optical switch matrix leading to the WDM devices, and wherein the connection verification system comprises:

a first selection unit for controllably extracting single-carrier input signals from among the signals leading from the outputs of the wavelength converting switch;

a second selection unit for controllably extracting single-carrier switched signals from among the signals leading from the outputs of the WDM devices; and

a verification unit connected to the first and second selection units, for controlling operation of the first and second selection units as a function of said sub-maps and performing relative-delay-dependent signal processing operations on the signals extracted by the selection units so as to identify connections established by each optical switch matrix and to determine their consistency with the associated sub-map.

31. A switch as claimed in claim 28, wherein the connection verification system is coupled to the inputs of the WDD devices and to those outputs of each optical switch matrix connected to inputs of the wavelength converting switch.

32. A switch as claimed in claim 31, wherein the connection map is defined by a set of sub-maps including a sub-map for

each optical switch matrix defining a desired interconnection pattern between the inputs of that optical switch matrix leading from the WDD devices and the outputs of that optical switch matrix leading to the wavelength converting switch, and wherein the connection verification system comprises:

a first selection unit for controllably extracting single-carrier input signals from among the signals leading from the outputs of the WDD devices;

a second selection unit for controllably extracting single-carrier switched signals from among the signals leading to the inputs of the wavelength converting switch; and

a verification unit connected to the first and second selection units, for controlling operation of the first and second selection units as a function of said sub-maps and performing relative-delay-dependent signal processing operations on the signals extracted by the selection units so as to identify connections established by each optical switch matrix and to determine their consistency with the associated sub-map.

33. A switch as claimed in claim 28, wherein the connection verification system is coupled to the inputs and outputs of the wavelength converting switch.

34. A switch as claimed in claim 33, wherein the connection map is defined by a set of sub-maps including a sub-map defining a desired interconnection pattern between the inputs and outputs of the wavelength converting switch, and wherein the connection verification system comprises:

a first selection unit for controllably extracting single-carrier input signals from among the signals leading to the inputs of the wavelength converting switch;

a second selection unit for controllably extracting single-carrier switched signals from among the signals leading from the outputs of the wavelength converting switch; and

a verification unit connected to the first and second selection units, for controlling operation of the first and second selection units as a function of said sub-map and performing relative-delay-dependent signal processing operations on the signals extracted by the selection units so as to identify connections established by the wavelength converting switch and to determine their consistency with said sub-map.

35. A switch as claimed in claim 33, wherein the wavelength converting switch has an additional plurality of inputs for accommodating a plurality of add carriers.

36. A switch as claimed in claim 35, wherein the connection map is defined by a set of sub-maps including a sub-map defining a desired interconnection pattern between the additional inputs of the wavelength converting switch and those outputs of the wavelength converting switch leading to inputs of the optical switch matrices, and wherein the connection verification system comprises:

a first selection unit for controllably extracting single-carrier input signals from among the add carriers;

a second selection unit for controllably extracting single-carrier switched signals from among the signals leading to the inputs of the optical switch matrices; and

a verification unit connected to the first and second selection units, for controlling operation of the first and second selection units as a function of said sub-map and performing relative-delay-dependent signal processing operations on the signals extracted by the selection units so

as to identify connections established by the wavelength converting switch and to determine their consistency with said sub-map.

37. A switch as claimed in claim 33, wherein the wavelength converting switch has an additional plurality of outputs for accommodating a plurality of drop carriers.

38. A switch as claimed in claim 37, wherein the connection map is defined by a set of sub-maps including a sub-map defining a desired interconnection pattern between those inputs of the wavelength converting switch leading from the optical switch matrices and the additional outputs of the wavelength converting switch, and wherein the connection verification system comprises:

a first selection unit for controllably extracting single-carrier input signals from among the signals leading from the outputs of ht optical switch matrices;

a second selection unit for controllably extracting single-carrier switched signals from among the drop carriers; and

a verification unit connected to the first and second selection units, for controlling operation of the first and second selection units as a function of said sub-map and performing relative-delay-dependent signal processing operations on the signals extracted by the selection units so as to identify connections established by the wavelength converting switch and to determine their consistency with said sub-map.

39. A switch as claimed in claim 27, wherein the first selection unit allows selection of an input signal as a function of its wavelength and position among the inputs of the optical switch matrix at that wavelength.

40. A switch as claimed in claim 39, wherein the first selection unit comprises:

a plurality of first local WDD devices for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices;

a bank of optical receivers connected to the outputs of the first local WDD devices, for converting the respective optical signals into electrical form;

a plurality of first selectors, each having a plurality of inputs, each such input on a given selector being associated with an output from a different one of the first local WDD devices and thereby permitting wavelength selection; and

a second selector connected to an output of each of the first selectors, thereby permitting selection of the position of the input of the optical switch matrix in the switching core.

41. A switch as claimed in claim 39, wherein the first selection unit comprises:

a local optical switch matrix for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices and selectively providing one of these multi-carrier signals to an output, thereby permitting selection of the position of the input of the optical switch matrix in the switching core;

a local WDD device connected to the output of the local optical switch matrix, for separating the received multi-carrier optical signal into its single-carrier components;

a bank of optical receivers connected to the outputs of the local WDD device, for converting the respective optical signals into electrical form; and

a selector connected to an output of each of the optical receivers, thereby permitting wavelength selection.

42. A switch as claimed in claim 39, wherein the first selection unit comprises:

a first local optical switch matrix for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices and selectively providing one of these multi-carrier signals to an output, thereby permitting selection of the position of the input of the optical switch matrix in the switching core;

a local WDD device connected to the output of the first local optical switch matrix, for separating the received multi-carrier optical signal into its single-carrier components;

a second local optical switch matrix for receiving the plurality of single-carrier optical signals from the local WDD device and selectively providing one of these multi-carrier signals to an output, thereby permitting wavelength;

an optical receiver connected to the output of the second local optical switch matrix, for converting the received optical signal into electrical form.

43. A switch as claimed in claim 39, wherein the first selection unit comprises:

a bank of tunable optical filters, for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices and selectively filtering these multi-carrier signals, thereby permitting wavelength selection;

a bank of optical receivers, each connected to the output of a respective one of the tunable optical filters, for converting the respective optical signal into electrical form; and

a selector connected to an output of each of the optical receivers, thereby permitting selection of the position of the input port in the optical switching matrix in the switching core.

44. A switch as claimed in claim 39, wherein the first selection unit comprises:

a local optical switch matrix for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices and selectively providing one of these multi-carrier signals to an output, thereby permitting selection of the position of the input of the optical switch matrix in the switching core;

a tunable optical filter, for selectively filtering the multi-carrier optical signal received from the local optical switch matrix, thereby permitting wavelength selection; and

an optical receiver connected to an output of the tunable optical filter, for converting the received optical signal to electrical form.

45. A switch as claimed in claim 39, wherein the second selection unit comprises:

a plurality of first local WDD devices for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices;

a bank of optical receivers connected to the outputs of the first local WDD devices, for converting the respective optical signals into electrical form;

a plurality of first selectors, each having a plurality of inputs, each such input on a given selector being associated with an output from a different one of the first local WDD devices and thereby permitting wavelength selection; and

a second selector connected to an output of each of the first selectors, thereby permitting selection of the position of the input of the optical switch matrix in the switching core.

46. A switch as claimed in claim 39, wherein the second selection unit comprises:

a local optical switch matrix for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices and selectively providing one of these multi-carrier signals to an output, thereby permitting selection of the position of the input of the optical switch matrix in the switching core;

a local WDD device connected to the output of the local optical switch matrix, for separating the received multi-carrier optical signal into its single-carrier components;

a bank of optical receivers connected to the outputs of the local WDD device, for converting the respective optical signals into electrical form; and

a selector connected to an output of each of the optical receivers, thereby permitting wavelength selection.

47. A switch as claimed in claim 39, wherein the second selection unit comprises:

a first local optical switch matrix for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices and selectively providing one of these multi-carrier signals to an output, thereby permitting selection of the position of the input of the optical switch matrix in the switching core;

a local WDD device connected to the output of the first local optical switch matrix, for separating the received multi-carrier optical signal into its single-carrier components;

a second local optical switch matrix for receiving the plurality of single-carrier optical signals from the local WDD device and selectively providing one of these multi-carrier signals to an output, thereby permitting wavelength;

an optical receiver connected to the output of the second local optical switch matrix, for converting the received optical signal into electrical form.

48. A switch as claimed in claim 39, wherein the second selection unit comprises:

a bank of tunable optical filters, for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices and selectively filtering these multi-carrier signals, thereby permitting wavelength selection;

a bank of optical receivers, each connected to the output of a respective one of the tunable optical filters, for converting the respective optical signal into electrical form; and

a selector connected to an output of each of the optical receivers, thereby permitting selection of the position of the input port in the optical switching matrix in the switching core.

49. A switch as claimed in claim 39, wherein the second selection unit comprises:

a local optical switch matrix for receiving a plurality of multi-carrier optical signals tapped prior to entering the first WDD devices and selectively providing one of these multi-carrier signals to an output, thereby permitting selection of the position of the input of the optical switch matrix in the switching core;

a tunable optical filter, for selectively filtering the multi-carrier optical signal received from the local optical switch matrix, thereby permitting wavelength selection; and

an optical receiver connected to an output of the tunable optical filter, for converting the received optical signal to electrical form.

50. A switch as claimed in claim 27, wherein the verification unit is operable to:

coordinate operation of the first and selection units such that the switched signal extracted by the second selection unit is expected to be correlated with the input signal extracted by the first selection unit

process the single-carrier input signal extracted by the first selection unit and the single-carrier switched signal extracted by the second selection unit in order to determine a level of correlation or anti-correlation therebetween; and

if the level of correlation is significant or the level of anti-correlation is insignificant, concluding that the connection involving the extracted input signal is consistent with the connection map.

51. A switch as claimed in claim 50, the verification unit being further operable to perform the step of:

if the level of correlation is insignificant or the level of anti-correlation is significant:

(1) coordinating operation of the first and selection units such that the switched signal extracted by the second selection unit is expected not to be correlated with the input signal extracted by the first selection unit;

(2) processing the pair of extracted signals to determine the level of correlation or anti-correlation therebetween;

(3) if the level of correlation is significant or the level of anti-correlation is insignificant, concluding that said input signal has been mis-connected; otherwise:

(3.1) if all switched signals not expected to be correlated with said input signal have been exhausted, concluding that the connection involving said input signal has been lost; otherwise:

(3.1.1) coordinating operation of the first and second selection units such that a different switched signal extracted by the second selection unit is expected not to be correlated with the input signal extracted by the first selection unit and repeating steps (2) and (3).

52. A switch as claimed in claim 51, wherein the verification unit comprises:

a first sampling unit for sampling the input signal extracted by the first selection unit, thereby to create a first sample stream;

a second sampling unit for sampling the switched signal extracted by the second selection unit, thereby to create a second sample stream;

a first delay line for receiving the first sample stream, comprising a plurality of taps interspersed by delay elements;

a second delay line for receiving the second sample stream, comprising a plurality of taps interspersed by delay elements;

a plurality of anti-correlators, each having a first input connected to a tap in the first delay line and a second input connected to a tap in the second delay line, each correlator being adapted to produce an anti-correlation value at a distinct relative delay; and

a minimum detector connected to the anti-correlators, for selecting the least among the anti-correlation values produced by the anti-correlators and providing the result to a controller.

53. A system as claimed in claim 52, wherein the first and second sampling units each comprise an anti-alias filter, a sampler and an analog-to-digital converter.

54. A system as claimed in claim 52, wherein each anti-correlator is adapted to produce an anti-correlation value that is a function of the difference between the values of the samples appearing at its first and second inputs.

55. A system as claimed in claim 52, wherein each anti-correlator is adapted to produce an anti-correlation value from an input signal x(i) and a switched signal y(i) that is substantially equal to a moving average value of $(x(i-s)-y(i))^2$, where "s" represents a constant relative delay between the two signals.

56. A system as claimed in claim 51, wherein the verification unit comprises:

a first sampling unit for sampling the input signal extracted by the first selection unit, thereby to create a first sample stream;

a second sampling unit for sampling the switched signal extracted by the second selection unit, thereby to create a second sample stream;

a first delay line for receiving the first sample stream, comprising a plurality of taps interspersed with delay elements;

a second delay line for receiving the second sample stream, comprising a plurality of taps interspersed with delay elements;

a plurality of correlators, each having a first input connected to a tap in the first delay line and a second input connected to a tap in the second delay line, each correlator being adapted to produce a correlation value; and

a maximum detector connected to the correlators, for selecting the greatest among the correlation values produced by the correlators and providing the result to a controller.

57. A system as claimed in claim 56, wherein the first and second sampling units each comprise an anti-alias filter, a sampler and an analog-to-digital converter.

58. A system as claimed in claim 27, wherein all single-carrier optical signals are digitally wrapped and include a header, wherein the header is designed to contain specific low-frequency signal content.

59. In combination, the switch of claim 25 and a power spectrum flattening system.

60. In combination, the switch of claim 27 and a power spectrum flattening system, wherein at least part of the first or second selection unit is shared between the switch and the power spectrum flattening system.

61. A system for correlating a first sample stream with a second sample stream, comprising:

a first delay line for receiving the first sample stream, comprising a plurality of taps interspersed by delay elements;

a second delay line for receiving the second sample stream, comprising a plurality of taps interspersed by delay elements;

a plurality of anti-correlators, each having a first input connected to a tap in the first delay line and a second input connected to a tap in the second delay line, each correlator being adapted to produce an anti-correlation value at a distinct relative delay; and

a minimum detector connected to the anti-correlators, for selecting the least among the anti-correlation values produced by the anti-correlators and providing the result to a controller.

62. A system as claimed in claim 61, wherein the first and second sampling units each comprise an anti-alias filter, a sampler and an analog-to-digital converter.

63. A system as claimed in claim 61, wherein each anti-correlator is adapted to produce an anti-correlation value that is a function of the difference between the values of the samples appearing at its first and second inputs.

64. A system as claimed in claim 61, wherein each anti-correlator is adapted to produce an anti-correlation value from an input signal x(i) and a switched signal y(i) that is substantially equal to a moving average value of $(x(i-s)-y(i))^2$, where "s" represents a constant relative delay between the two signals.

65. A system as claimed in claim 61, wherein each anti-correlator is uniquely associated with a relative delay existing between the sample streams at its first and second inputs.

66. A system as claimed in claim 64, wherein for each particular anti-correlator, at least one other of the anti-correlators is associated with a relative delay that is within "x" seconds of the relative delay with which said particular anti-correlator is associated, "x" being substantially the inverse of the highest frequency contained in the first or second sample stream.

67. A system as claimed in claim 61, wherein each tap in the first and second delay lines is connected to at most one of said anti-correlators.

68. A system as claimed in claim 61, wherein at least one tap in the first or second delay line is connected to more than one of said anti-correlators.

69. A system as claimed in claim 61, wherein the delay elements are embodied as shift registers.